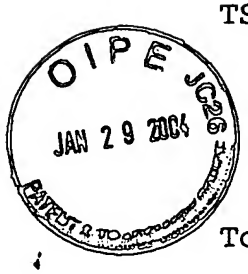
TSMC-02-1089



January 6, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/694,676 10/28/03 |

Tao-Ping Wang

HIGH EFFICIENCY REDUNDANCY ARCHITECTURE IN SRAM COMPILER

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 1/27/04

U.S. Patent 5,742,556 to Tavrow et al., "Redundancy Scheme for Semiconductor RAMs," describes a redundancy scheme for semiconductor RAMs.

U.S. Patent 5,612,918 to McClure, "Redundancy Architecture," describes redundancy architecture that reduces the complexity of the redundancy structure because it has fewer pass gates in the redundant decoder.

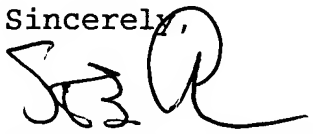
U.S. Patent 5,257,229 to McClure et al., "Column Redundancy Architecture for a Read/Write Memory," describes a column redundancy architecture for a read/write memory whereby an integrated circuit memory has its primary memory array arranged into blocks with redundant columns.

U.S. Patent 5,134,584 to Boler et al., "Reconfigurable Memory," describes a configurable device that uses a plurality of parallel units that are made up of cells for storing individual bits of information.

U.S. Patent 4,807,191 to Flannagan, "Redundancy for a Block-Architecture Memory," describes redundancy for block-architecture memory.

U.S. Patent 4,691,301 to Anderson, "Semiconductor Memory with Redundant Column Circuitry," describes a semiconductor memory with redundant column circuitry that includes a row of shared predecoder and predecoders.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-1089	10/694,676
Applicant: Tao-Ping Wang	
Filing Date: 10/28/03	Group Art Unit

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	5,742,556	4/21/98	Tavrow et al.	365	225.7	12/26/96
	5,612,918	3/18/97	McClure	365	200	12/29/95
	5,257,229	10/26/93	McClure et al.	365	200	1/31/92
	5,134,584	7/28/92	Boler et al.	365	200	7/22/88
	4,807,191	2/21/89	Flannagan	365	189	1/4/88
	4,691,301	9/1/87	Anderson	365	200	6/20/86

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

TSMC-02-1089

January 6, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/694,676 10/28/03

Tao-Ping Wang

HIGH EFFICIENCY REDUNDANCY ARCHITECTURE IN SRAM COMPILER

ASSOCIATE POWER OF ATTORNEY

I hereby appoint Billy Knowles, registration number 42,752, as my associate attorney in this case. His telephone number is (845) 331-3866.

Please continue to direct all correspondence in this case to the undersigned attorney.

Respectfully submitted,

Stephen B. Ackerman,

Principal attorney of record